IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	**MAIL STOP AF**
Gregory S. Andre	Group Art Unit: 2112
Application No.: 09/955,961	Examiner: Christopher E. Lee
Filed: September 20, 2001	Confirmation No.: 1901
For: TWO LEVEL MULTI-TIER SYSTEM BUS	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the final Office Action dated April 26, 2006, a Notice of Appeal is filed herewith, and a Pre-Appeal Conference is requested to review the above-identified application. No amendments are being filed with this request. For at least the following reasons, the rejections raised in the Final Office Action are clearly improper and without basis.

OVERVIEW

Independent claims 1 and 17 are allowable over JP 409022380 A (Kimura); U.S. Patent 6,842,800 (Dupont); JP 408272756 A (Yamagami et al.); and U.S. Patent 5,502,718 (Lane et al.). These documents, when considered individually or in the combination suggested by the Examiner, do not teach or suggest at least the Applicants' claimed features of: "a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system

bus," as recited in claim 1, and as similarly recited in claim 17. Independent claims 1 and 17 are therefore allowable.

ARGUMENT

1. The Examiner Has Failed To Establish A Prima Facie Case of Obviousness In Combining The Kimura Publication; The Dupont Patent; The Yamagami et al. Publication; and The Lane et al. Patent To Reject Independent Claims 1 And 17.

Applicants have disclosed a method and apparatus for managing flow of information among plural processors of a processing array. The flow of data and control packet information is managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraphs [0027] and [0028]). The system bus 102 is the primary control and data path of the processor subsystem (e.g., paragraph [0027]). A system bus arbitration unit 112 of the system controller is provided for arbitrating access to the system bus by the various modules (e.g., paragraph [0026]). As exemplified in Fig. 9, packet buffers are separately maintained, such as a direct memory access (DMA) packet FIFO buffer 906 and a control action (CA) FIFO buffer 914 for transmission, and DMA packet FIFO buffer 912 and a control action packet FIFO buffer 910 for reception, even though they access a common system bus. Control action packet FIFO buffers (910 and 914) are maintained separate from the DMA packet FIFO buffers (906 and 912) (e.g., specification at paragraph [00136]). Accordingly, control action operations can bypass a DMA packet FIFO buffer for bus access (e.g., specification at paragraph [00152]).

None of the documents relied upon by the Examiner, considered alone or in combination, teach or suggest: a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus, as recited in independent claims 1, and as similarly recited in claim 17.

On page 3 of the Office Action, the Examiner admits that the Kimura publication does not teach said path being for "packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus," as recited in claim 1, and as similarly recited in claim 17.

The Dupont patent does not cure the deficiencies of the Kimura publication. The Examiner asserted at page 3 of the final Office Action that the Dupont patent discloses that a buffer is "separately connected between a respective local processor bus and a system bus." Applicant respectfully disagrees. Col. 4, lines 16-23 of the Dupont patent as relied upon by the Examiner actually discloses "[r]eferring now to FIG. 2, a diagram of a preferred buffer storage section 50 is shown. The buffer storage section 50 has been sub-divided to include two buffer storage subsections, subsection 90 and subsection 100. Subsection 90 includes a plurality of buffer units of size s and subsection 100 includes a plurality of buffer units of size b. Subsection 90 has N buffer units thereby forming a buffer subsection of size Ns. Subsection 100 has M buffer units thereby forming a buffer subsection of size Mb." The Dupont patent makes no mention of control information packets being separately buffered in a buffer separately connected between a local processor bus and a system bus.

The Dupont patent does not teach or suggest "a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus," as recited in claim 1, and as similarly recited in claim 17.

The Yamagami et al. publication does not cure the deficiencies of the Kimura publication and the Dupont patent. The Yamagami et al. publication was applied for its disclosure of a boot process for a multiprocessor system involving arbitrated bus access according to a priority based rule. However, the Yamagami publication does not teach or suggest the recited claim features.

The Lane et al. patent does not cure the deficiencies of the Kimura publication, the Dupont patent and the Yamagami et al. publication. The Lane et al. patent shows in Fig. 2 data packets exchanged through paths 26, 27 (col. 6, lines 47-60) that are separate and distinct from the command information paths 211, 214, 215. Further, the Lane et al. disclosure does not teach or suggest that these command information paths 211, 214, 215 transfer packets. At least for the foregoing reasons, the Lane et al. patent does not cure the deficiencies of the Kimura publication, the Dupont patent, and the Yamagami et al. publication.

The Sand et al. patent, the Shanley et al. article, and the McDonald et al. patent were secondary references relied upon by the Examiner to reject certain dependent claims in various combinations with the aforementioned references. Accordingly, these other references do not teach or suggest the recited claim features.

2. The Dupont Patent Is Not Prior Art.

The Dupont patent was filed on August 30, 2001. Although the present application was filed on September 20, 2001, the attached copies of Applicant's Declaration and Assignment were both signed by the Applicant on August 2, 2001. Accordingly, Applicant submits that the present application is a prior invention before the filing date of the Dupont patent. The Dupont patent is not prior art.

At least for the reasons as set forth above, claims 1 and 17 are therefore allowable. All of the remaining claims depend from independent claims 1 and 17 and recite additional advantageous features which further distinguish over the applied references.

CONCLUSION

The Examiner has not established a prima facie case of obviousness in combining the applied references to reject claims 1-31. A reversal of the final rejection, and allowance of the present application, are therefore requested.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: July 25, 2006

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for Patrick C. Keane
Registration No. 32858

Attached:
Copy of Declaration dated August 2, 2001
Copy of Assignment dated August 2, 2001

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